first and second channel regions having width directions essentially perpendicular to each other,

a first source electrode and a first drain electrode, adjacent to the first and second channel regions and opposing each other with the first and second channel regions therebetween, and in ohmic contact with the active region,

a first gate electrode on the first and second channel regions and along the first source electrode and the first drain electrode, and bent at at least one bending position; and

a fifth channel region joining the second channel region and having a width direction essentially perpendicular to the width direction of the second channel region, wherein the first gate electrode is disposed on the first, second, and fifth channel regions and is bent at the first bending position and at a third bending position; and

(d) a second semiconductor element on the active region adjacent to the first semiconductor element, including

third and fourth channel regions adjacent to the first and second channel regions, respectively, with one of the first source electrode and the first drain electrode therebetween,

one of a second source electrode and a second drain electrode opposing the first drain electrode or the first source electrode across the third and fourth channel regions, and in ohmic contact with the active region,

a second gate electrode on the third and fourth channel regions and along one of the second source electrode and the second drain electrode, and bent at at least one bending position; and

a sixth channel region joining the fourth channel region and having a width direction essentially perpendicular to the width direction of the fourth channel region, wherein the second gate electrode is disposed on the third, fourth, and sixth channel regions and is bent at the second bending position and at a fourth bending position; and

(e) first and second insulating regions on the semiconductor substrate and under the first and second bending positions of the first and second gate electrodes, and under the third and fourth bending positions of the first and second gate electrodes, respectively.

6. (Thrice Amended) A semiconductor device comprising:

(a) an electrically isotropic compound semiconductor substrate having a first surface and a second surface;

(b) an active region on the first surface of the substrate;

(c) a first semiconductor element in the active region, including

first and second channel regions having width directions essentially perpendicular to each other,

a first source electrode and a first drain electrode, adjacent to the first and second channel regions and opposing each other with the first and second channel regions therebetween, and in ohmic contact with the active region, wherein the first source electrode has a rectangular shape, two sides of which are adjacent to the first and second channel regions, respectively, and wherein the first source electrode is connected to a conductive film on the second surface of the semiconductor substrate through a via-hole in the first source electrode,

a first gate electrode on the first and second channel regions and along the first source electrode and the first drain electrode, and bent at at least one bending position; and

a fifth channel region joining the second channel region and having a width direction essentially perpendicular to the width direction of the second channel region, wherein the first gate electrode is disposed on the first, second, and fifth channel regions and is bent at the first bending position and at a third bending position; and

(d) a second semiconductor element on the active region adjacent to the first semiconductor element, including

third and fourth channel regions adjacent to the first and second channel regions, respectively, with one of the first source electrode and the first drain electrode therebetween,

one of a second source electrode and a second drain electrode opposing the first drain electrode or the first source electrode across the third and fourth channel regions, and in ohmic contact with the active region,

a second gate electrode on the third and fourth channel regions and along one of the second source electrode and the second drain electrode, and bent at at least one bending position; and

a sixth channel region joining the fourth channel region and having a width direction essentially perpendicular to the width direction of the fourth channel region, wherein the second gate electrode is disposed on the third, fourth, and sixth channel regions and is bent at the second bending position and at a fourth bending position; and

(e) first and second insulating regions on the semiconductor substrate and under the first and second bending positions of the first and second gate electrodes, and under the third and fourth bending positions of the first and second gate electrodes, respectively.

7. (Thrice Amended) The semiconductor device according to claim 6, wherein the width of one of the first and second channel regions is narrower than the width of the source electrode adjacent the channel region.